

10/535273  
13

IC14 Rec'd PCT/PTO 17 MAY 2005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): **OTOMO ET AL.**) Conf. No.: \_\_\_\_\_

Appln No.: **Not Yet Assigned**) \_\_\_\_\_

Filed: **Herewith**) **CERTIFICATE OF MAILING BY "EXPRESS MAIL"**

For: **PHASE COMPARATOR CIRCUIT**  
**AND CDR CIRCUIT**) "Express Mail" Mailing Label Number  
\_\_\_\_\_  
EV 513605049 US

Group Art Unit: **Not Yet Assigned**) Date of Deposit May 17, 2005

Examiner: **Not Yet Assigned**) I hereby certify that this paper or fee is being deposited with the  
United States Postal Service "Express Mail Post Office to  
Addressee" Service under 37 CFR §1.10 on the date indicated  
above and is addressed to the Mail Stop PCT, Commissioner for  
Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

---

Docket No.: **85366**) Ed Price  
(Typed or printed name of person mailing)  


Cust. No.: **22242**) (Signature of person mailing) \_\_\_\_\_

INFORMATION DISCLOSURE STATEMENT

Mail Stop PCT  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §§1.97 and 1.98, applicant and the undersigned attorney wish to bring the following information to the Examiner's attention in connection with the examination of the above-captioned application.

The documents are listed on PTO/SB/08A Substitute for Form PTO-1449 which accompanies this Information Disclosure Statement. A copy of each foreign document and each non-patent literature document cited thereon is enclosed herewith.

U.S. PATENT DOCUMENTS		
Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
Number-Kind Code <sup>2</sup>		
US-6,225,831 B1	05/01/2001	Dalmia et al.
US-6,421,404 B1	07/16/2002	Nakamura
US-2003/0142774 A1	07/31/2003	Takasoh et al.

10/535273

JC14 Re/PCT/PTO 17 MAY 2005  
Attorney Docket No. 85366

## Information Disclosure Statement

FOREIGN PATENT DOCUMENTS		
Foreign Patent Document Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup>	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
JP2000077990	03/14/2000	Victor Co. of Japan Ltd.
JP2001144592	05/25/2001	Fujitsu Ltd.
JP2002171160	06/14/2002	Nec Eng Ltd.

NON PATENT LITERATURE DOCUMENTS
Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
NAKAMURA, KAZUYUKI; FUKAISHI, MUNEO; ABIKO, HITOSHI; MATSUMOTO, AKIRA and YOTSUYANAGI, MICHIO, A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock, IEEE, 1998
SAVOJ, JAFAR and RAZAVI, BEHZAD, A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector, IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, May 2001, pages 761-768.
OHTOMO, YUSUKE; KAWAMURA, TOMOAKI; NISHIMURA, KAZUYOSHI, NOGAWA, MASAFUMI; KOIZUMI, HIROSHI and TOGASHI, MINOURU, A 12.5 Gb/s CMOS BER Test Using A Jitter-Tolerant Parallel CDR, IEEE International Solid-State Circuits Conference, ISSCC Digest of Technical Papers, Feb. 2004, pages 174-175.

**R E M A R K S**

Pursuant to 37 CFR § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to be an admission that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 CFR § 1.56(b).

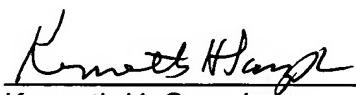
It is respectfully requested that the Examiner consider the above materials and make them of record in the above-captioned application.

The Commissioner is hereby authorized to charge any fees which may be required in this application under 37 C.F.R. § §1.16-1.17 to Deposit Account No. 06-1135.

Respectfully submitted,

FITCH, EVEN, TABIN & FLANNERY

Dated:

  
\_\_\_\_\_  
Kenneth H. Samples  
Registration No. 25,747

FITCH, EVEN, TABIN & FLANNERY  
120 South LaSalle Street  
Suite 1600  
Chicago, Illinois 60603-3406  
Telephone: (312) 577-7000  
Facsimile: (312) 577-7007

<b>PTO/SB/08a</b> Substitute for Form 1449A/PTO  <b>INFORMATION DISCLOSURE</b> <b>STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>				Application Number	Not Yet Assigned
				Filing Date	Herewith
				First Named Inventor	Otomo et al.
				Art Unit	Not Yet Assigned
				Examiner Name	Not Yet Assigned
				Sheet	1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup>			
		US-6,225,831 B1	05/01/2001	Dalmia et al.	
		US-6,421,404 B1	07/16/2002	Nakamura	
		US-2003/0142774 A1	07/31/2003	Takasoh et al.	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup>			
		JP2000077990	03/14/2000	Victor Co. of Japan Ltd.	X
		JP2001144592	05/25/2001	Fujitsu Ltd.	X
		JP2002171160	06/14/2002	Nec Eng Ltd.	X

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
		T <sup>2</sup>			
		NAKAMURA, KAZUYUKI; FUKAISHI, MUNEO; ABIKO, HITOSHI; MATSUMOTO, AKIRA and YOTSUYANAGI, MICHIO, A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock, IEEE, 1998			
		SAVOJ, JAFAR and RAZAVI, BEHZAD, A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector, IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, May 2001, pages 761-768.			
		OHTOMO, YUSUKE; KAWAMURA, TOMOAKI; NISHIMURA, KAZUYOSHI, NOGAWA, MASAFUMI; KOIZUMI, HIROSHI and TOGASHI, MINOURU, A 12.5 Gb/s CMOS BER Test Using A Jitter-Tolerant Parallel CDR, IEEE International Solid-State Circuits Conference, ISSCC Digest of Technical Papers, Feb. 2004, pages 174-175.			

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kind Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.